Application Note MSAN-175
Performing Nibble and Dibit Switching with the MT90820 (LDX)

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1.0 Introduction

Dibit switching (2 bits per channel) is essential to the operation of adjunct ISDN equipment that is used to terminate ISDN lines at (CO) Central Offices where D-channel processing capability is non-existent. The 16Kb/s D-channels are collected and packed into a T1/T3 or E1/E3 transmission facility and sent to a CO capable of processing the D-channel data.

Nibble switching (4 bits per channel) is used in digital wireless communications and pair gain systems where 8-bit (64Kb/s) PCM (Pulse Code Modulation) data is compressed into 4-bit (32Kb/s) ADPCM (Adaptive Differential Pulse Code Modulation) data.

This application note illustrates the use of the MT90820 as a dibit or nibble switch.

2.0 Switching Configuration

The MT90820 switches 8-bit (64Kb/s) channels at data rates of 2.048, 4.096, and 8.192Mb/s. In both dibit and nibble applications the devices internal clock rate must be increased while a lower data rate is maintained on the serial streams. The following sections show how to configure the MT90820 in such applications.

2.1 Dibit Switching

In dibit switching the MT90820 is set to run in the 8.192Mb/s mode while the external ST-BUS streams are maintained at 2.048Mb/s. The device over-samples the input stream by a factor of four. Each bit of the 2.048Mb/s input data stream is stored in four consecutive bit locations. Thus each dibit is stored in a single memory location, one bit in the first nibble of memory and the other bit in the second nibble of memory. In this configuration the MT90820 will output one bit in four consecutive bit cells. (Four bit cells at 8.192Mb/s = one bit cell at 2.048Mbp/s.) Figures 1A-C show the channel mapping and the input/output timing when the MT90820 is operated in dibit switching mode.

If 8-bit switching (64Kbp/s channel) is required while operating in the dibit switching configuration, four consecutive dibits must be switched.

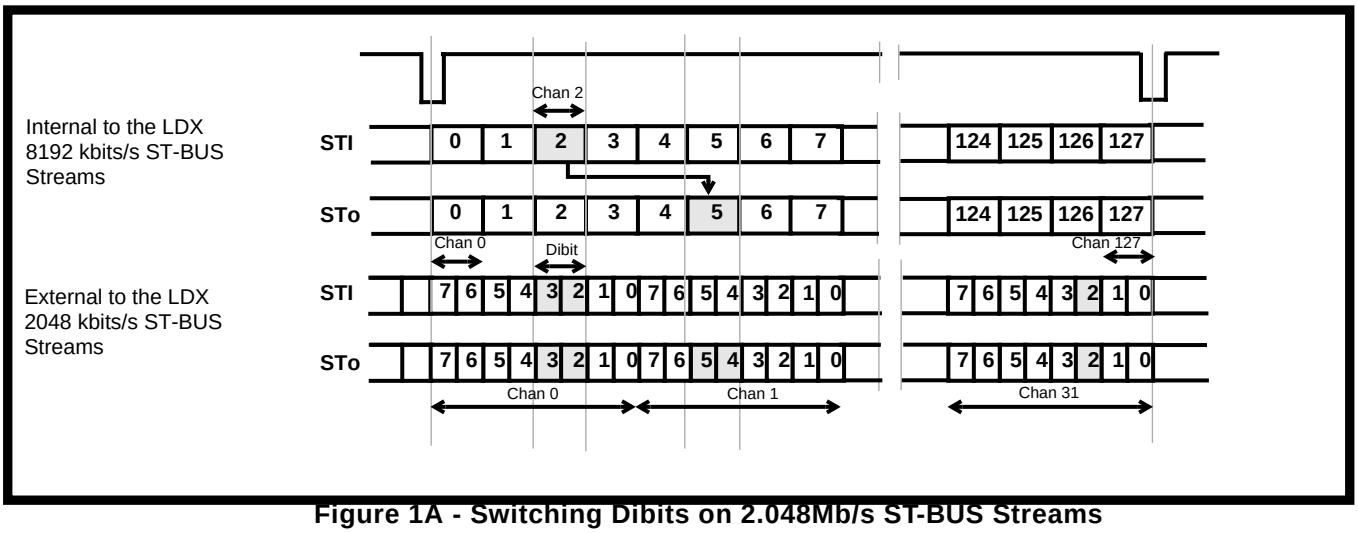

Figure 1A - Switching Dibits on 2.048Mb/s ST-BUS Streams

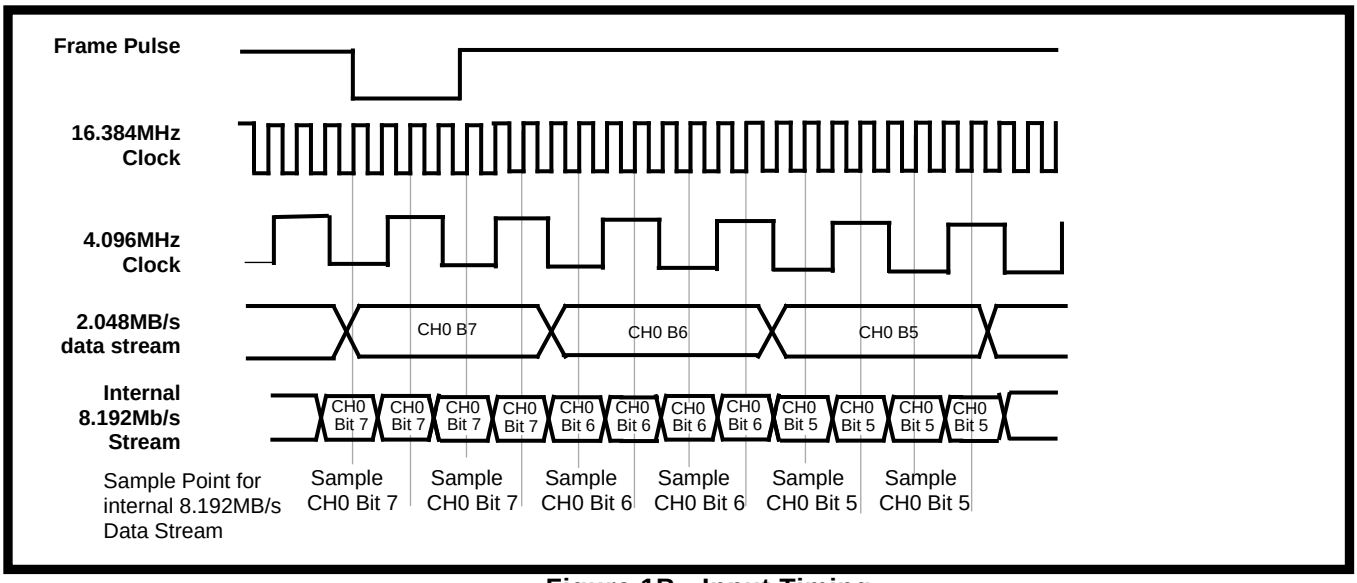

Figure 1B - Input Timing

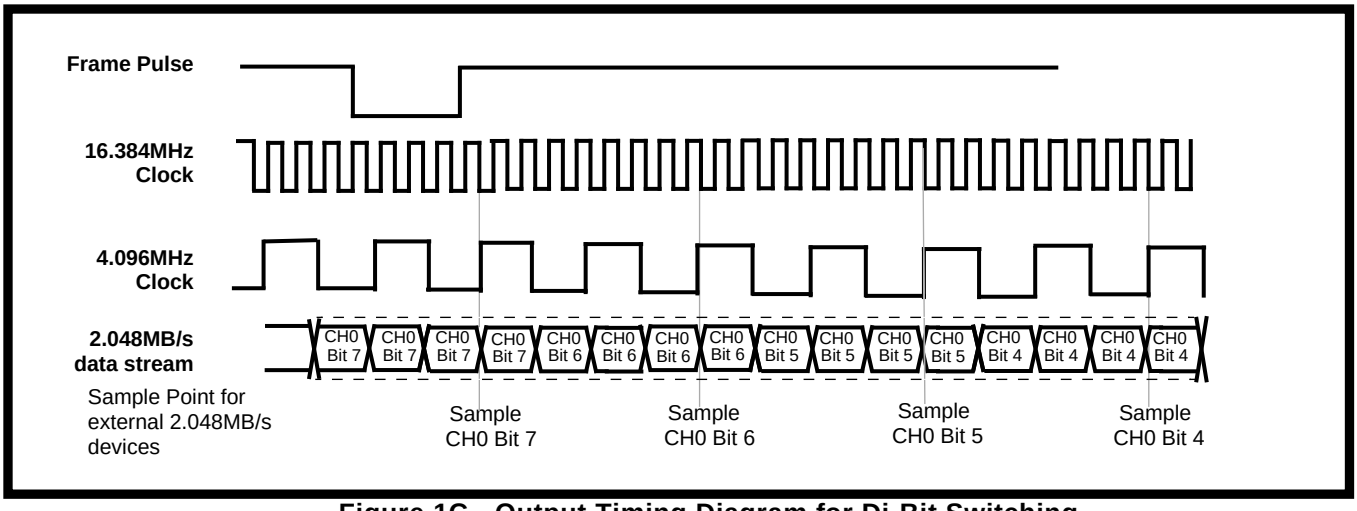

Figure 1C - Output Timing Diagram for Di-Bit Switching

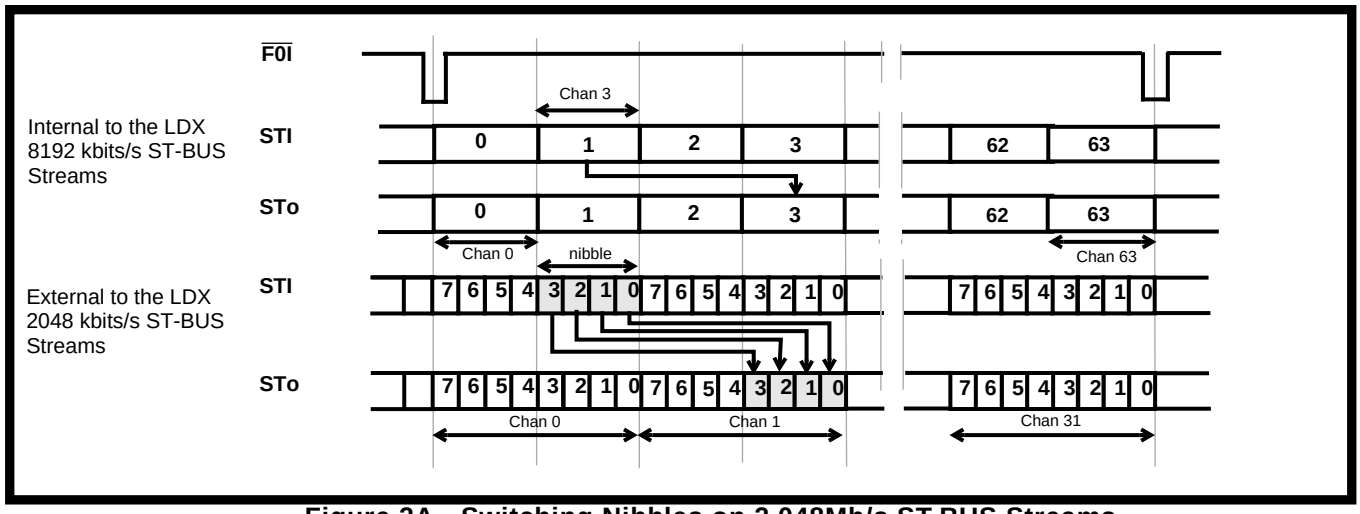

Figure 2A - Switching Nibbles on 2.048Mb/s ST-BUS Streams

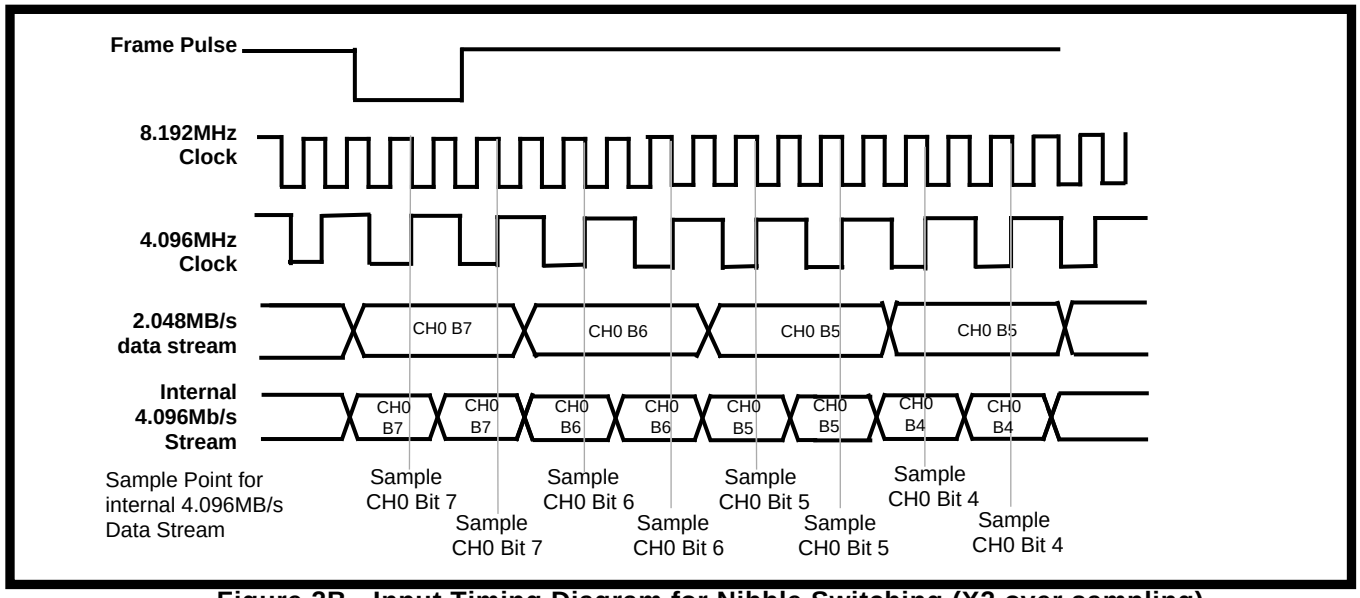

Figure 2B - Input Timing Diagram for Nibble Switching (X2 over sampling)

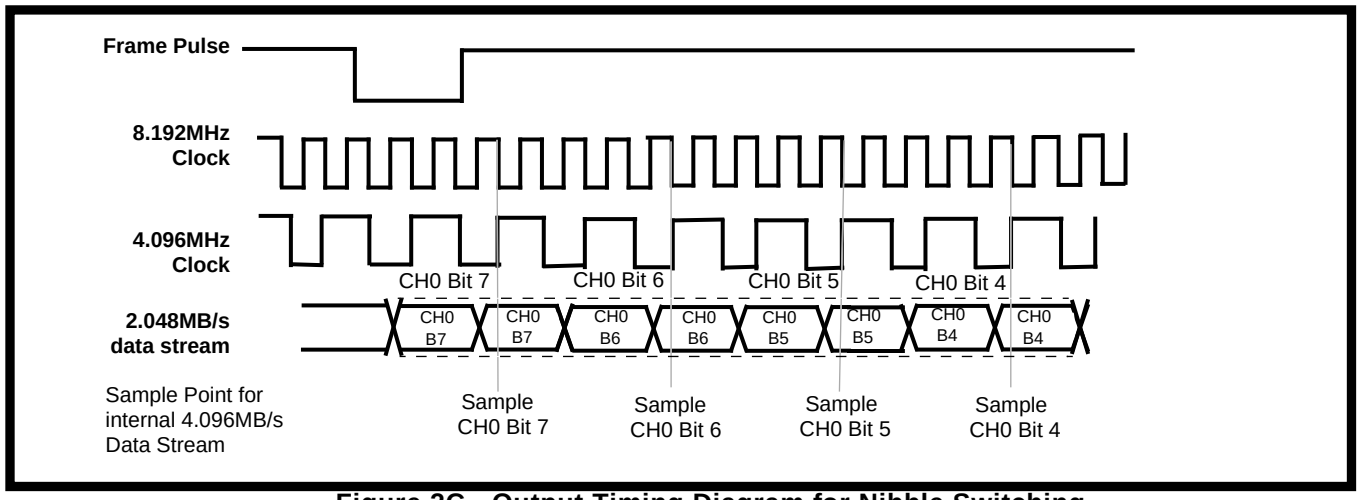

Figure 2C - Output Timing Diagram for Nibble Switching

2.2 Nibble Switching

In nibble switching the MT90820 is set to run in the 4.096Mbp/s mode while the external ST-BUS streams are maintained at 2.048Mbp/s. The device over-samples the input stream by a factor of two. Each bit of the 2.048Mbp/ data stream is stored in two consecutive bit locations. Thus each nibble is stored in one memory location (two bits in the first nibble of memory and two bits in the second nibble). In this configuration the MT90820 will output one bit in two consecutive bit cells (two bit cells at 4.096Mbp/s = one bit cell at 2/048Mbp/s). Figure 2 shows the channel mapping and the input/output timing for nibble mode.

If 8 bit switching (64Kbp/s channel) is required while operating in a nibble switching configuration, two consecutive nibbles must be switched.

3.0 Delay Constraints

When connecting digital devices, care must be taken to ensure that input timing requirements are met. These requirements may be violated from delays caused by loading of the output streams. As data rates increase, larger delays cannot be tolerated because the timing parameters become more rigorous. This is a consideration when over-sampling slower data streams, as is the case in dibit and nibble switching. See Figure 3.

3.1 Sampling offset adjustment

By default the MT90820 samples input data at the three-quarter point in the bit cell as shown in Figure 4. To compensate for bus delays, the input sampling point can be

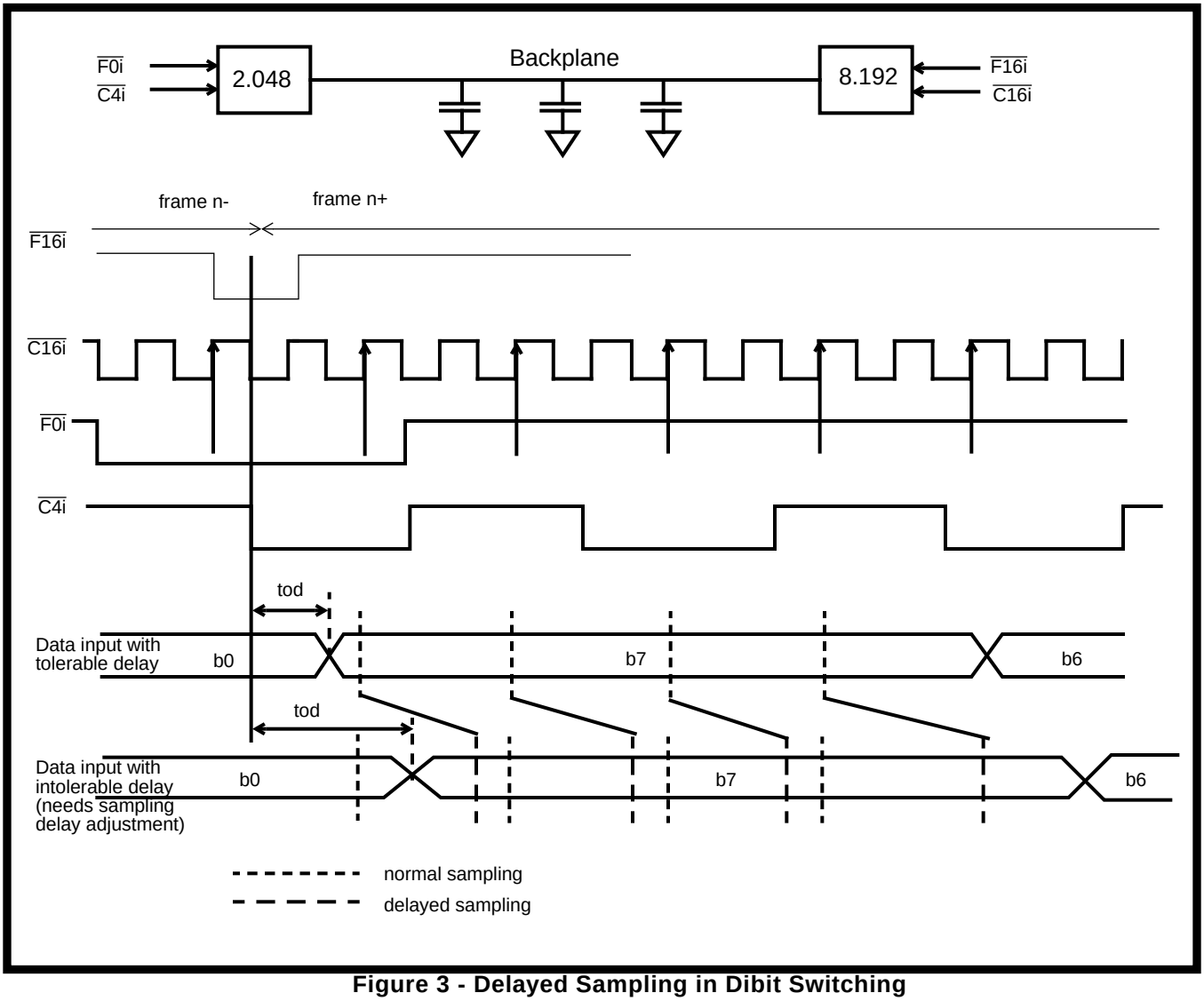

Figure 3 - Delayed Sampling in Dibit Switching

delayed by up to 4.5 clock cycles with a resolution of 0.5 clock cycles. The example shown in Figure 3A is a system with a bus delay equal to two clock cycles, a delay which would cause the device to incorrectly sample bit 0 instead of bit 7.Introducing a delay of 1.5 clock cycles realigns the sampling point with the delayed data stream.

3.2 Stream Delay Measurement

As explained in detail in the MT90820 data sheet, delay measurements of the input signal can be made with the MT90820 frame evaluation offset feature, or with software.

3.3 Software Algorithm

During steam delay measurement, the 2.048Mbp/s devices should be set to output a continuous bit pattern 0Chex on channel n where n is any channel. In dibit switching, channel n of the output device, running at 2.048Mbp/s, spans four consecutive input channels of the MT90820 running at 8.192Mbp/s, starting from channel 4 x n. These four channels should contain 0x00, 0x00, 0xFF and 0x00 if the timing parameters have been met. The algorithm given by the flow chart (Figure 5) will properly set the sampling point in the middle of the bit cell by measuring the minimum and maximum delay offsets (i, j respectively). Once I and j have been determined, the delay offset should be programmed to (i+j)/4) to provide optimum sampling of incoming bit cells.

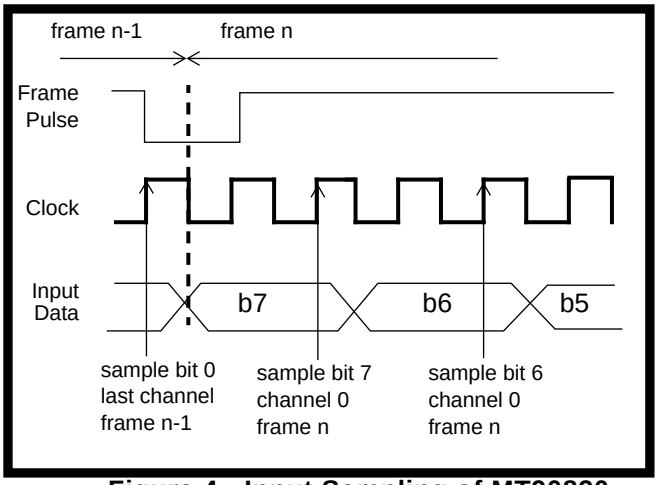

Figure 4 - Input Sampling of MT90820

4.0 Conclusion

In this application note we have illustrated the use of the MT90820 in dibit and nibble switching applications. We have also illustrated the devices per stream input delay feature which is particularly useful for managing large, multi-board systems that transport both voice channel and concatenated data channels over a backplane. We have also shown that the device can be used to measure stream delays. For more information consult the MT90820 Large Digital Switch data sheet, or contact your Mitel Semiconductor representative. On the internet reach us at www.mitelsemi.com/

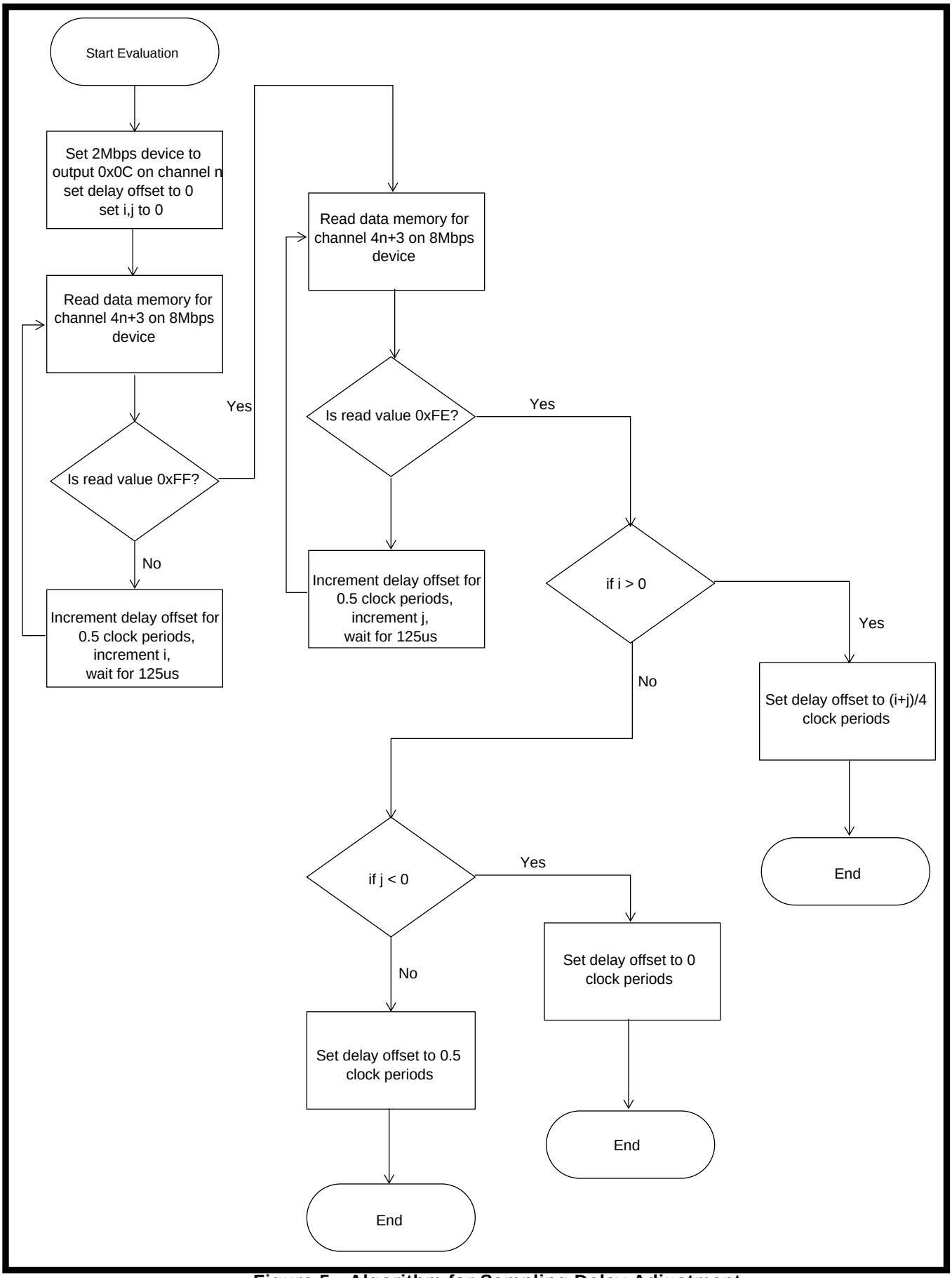

Figure 5 - Algorithm for Sampling Delay Adjustment

Notes:

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